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This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☑ This application has been examined ☑ Responsive to communication filed on July 28, 1995, Sept 15, 1995 and Oct. 10, 1995 ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), 0 days from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☑ Notice of References Cited by Examiner, PTO-892.
2. ☐ Notice of Draftsman's Patent Drawing Review, PTO-948.
3. ☑ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Patent Application, PTO-152.
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____.

Part II SUMMARY OF ACTION

1. ☑ Claims 1 - 127 are pending in the application.

   Of the above, claims _____ are withdrawn from consideration.

2. ☑ Claims 1 - 78 have been cancelled.

3. ☐ Claims _____ are allowed.

4. ☑ Claims 79 - 127 are rejected.

5. ☐ Claims _____ are objected to.

6. ☐ Claims _____ are subject to restriction or election requirement.

7. ☑ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.

8. ☐ Formal drawings are required in response to this Office action.

9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice of Draftsman's Patent Drawing Review, PTO-948).

10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____ has (have) been ☐ approved by the examiner; ☐ disapproved by the examiner (see explanation).

11. ☐ The proposed drawing correction, filed _____, has been ☐ approved; ☐ disapproved (see explanation).

12. ☐ Acknowledgement is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____; filed on _____.

13. ☐ Since this application apppears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.

14. ☐ Other

1. Claims 101-115 and 116-127 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 101-115:

At line 3, claim 101, the word "that" is repeated.

At line 13, claim 101, the phrase "said non-volatile memory sectors" lacks antecedent basis.

As per claim 105:

The phrase "the a" is not idiomatic.

As per claim 113:

The phrase "the spare cells portion" lacks antecedent basis.

As per claim 116-127:

At line 3, claim 116, the phrase "said memory system" lacks antecedent basis.

2. The above rationales for the rejection under 35 U.S.C. 112, second paragraph, are only exemplary examples indicating that the claims contain problems of indefiniteness. The Applicant is, hereby, requested to review each of the pending claims and correct all indefinite problems if found.

3. The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having

ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

4. Claims 85, 91, 101, 102 and 111 are rejected under 35 U.S.C. § 103 as being unpatentable over Burke (AU-B-22536/83) in view of Yorimoto et al (0-220-718 hereinafter referred to as Yorimoto).

As per claims 85, 91, 101, 102 and 111:

Burke teaches a computer system including (1) a processor and (2) a memory system. Burke's memory system includes an array of cells which are inherently partitioned into a plurality of sectors because Burke's array is to "emulate" a magnetic disk which has sectors. To operate his computer system, Burke provides the array, and a controller. Burke's controller is within a board and is for controlling the operation of the array. Burke's controller is caused, when it receives from the processor an address designating a sector of the magnetic disk. Burke's cells are written with information.

Yorimoto teaches partitioning the cells with a sector into portions, each portion is for storing a specific type of information.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use Yorimoto's memory (of EEPROM type) and Yorimoto's memory cells partitioning in place of Burke's memory.

The artisan would have been motivated to use Yorimoto's EEPROM in the place of Burke's memory because Yorimoto's EEPROM can be partitioned into sectors and Burke's

emulation inherently suggests that the emulating memory should be able to emulate the sectors of Burke's magnetic disk.

5. Claims 79-84, 86-90, 98-100, 103-105, 107-110, 112-115 are rejected under 35 U.S.C. § 103 as being unpatentable over Burke (AU-B-22536/83) in view of Yorimoto et al (0-220-718 hereinafter referred to as Yorimoto) and Satoh et al (4,774,700 hereinafter referred to as Satoh).

As per claim 79:

Burke teaches a computer system including (1) a processor and (2) a memory system. Burke's memory system includes an array of cells which are inherently partitioned into a plurality of sectors because Burke's array is to "emulate" a magnetic disk which has sectors. To operate his computer system, Burke provides the array, and a controller. Burke's controller is within a board and is for controlling the operation of the array. Burke's controller is caused, when it receives from the processor an address designating a sector of the magnetic disk. Burke's cells are written with information.

Yorimoto teaches partitioning the cells with a sector into portions, each portion is for storing a specific type of information.

Satoh teaches replacing of defective sector with usable sector. Satoh's sector replacing operation includes detecting of an unusable sector, linking the address of the unusable sector with the address of the usable sector, and accessing the usable sector.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use Yorimoto's memory (of EEPROM type) and Yorimoto's memory cells partitioning in place of Burke's memory and to apply Satoh's operation of sector replacing

to replace defective sector in Yorimoto's memory which has been used in the replace Burke's memory.

The artisan would have been motivated to use Yorimoto's EEPROM in the place of Burke's memory because Yorimoto's EEPROM can be partitioned into sectors and Burke's emulation inherently suggests that the emulating memory should be able to emulate the sectors of Burke's magnetic disk. The artisan would have also been motivated to use Satoh's operation of replacing defective sector in the modified memory system of Burke because the EEPROM replacing Burke's memory is prone to be defective and because Satoh's operation enhances fault tolerance.

As per claims 80 and 109:

Satoh teaches detecting a condition when a sector become defective.

As per claims 83, 87, 84, 103, 104 and 105:

It would have been obvious to one having ordinary skill in the art at the time the invention was made realize that addresses of defective sectors, error correction code and addresses of substitute sectors are information which can be written into (or read from) the overhead portions of a memory device.

As per claims 88 and 112:

Satoh's cells which are used for replacing his defective sectors are spare cells.

As per claims 82, 86 and 110:

The size of 512-bytes, which is took as a given amount of user data, is of obvious design choice.

As per claim 81 and 115:

Official notice is, hereby, taken that it is notoriously old and well known in the art to identify a bad group of cells, when the number of defective memory cells within the group of cells is greater than a preset number and the number of bit errors in the group of cells is beyond the capability of correcting by using error correction code, so that this group of cells can be replaced with an alternative group of cells.

As per claims 89, 98, 99, 90, 100, 106, 107, 108, 113 and 114:

Official notice is, hereby taken that:

a. linking the address of unusable sector with address of useable sector by storing address of corresponding useable sector,

b. identifying defective sector and storing addresses of defective sector, and

c. including, as overhead data, an identification of defective cells within the user data portion; and

d. accessing a usable sector by (1) referring to the useable sector address stored in the unusable sector and (2) referring to the list to translate the address of the unusable sector into an address of a usable sector,

e. causing the controller (1) to read the identification of defective cells and then (2) to substitute therefore other cells within the spare cell portion, and

f. designating an address of a sector by (1) substituting an address of another sector and (2) reading the address of a corresponding sector and then accessing data within such other sector

are notoriously old and well known in the art of memory patching.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate (1) those conventional features of address translation for

referring to useable sector (or cells) instead of defective sector (or cells) and (2) those conventional features of mapping unusable sector (or cells) into useable sector (or cells) into the modified system of Burke. The artisan would have been motivated to incorporate these memory patching features into the modified system of Burke because:

a Burke teaches (1) translating of address signals so as to access an alternative memory location instead of memory location which is to be avoided and (2) emulating a magnetic memory by using a semiconductor memory;

b semiconductor memories (e.g. Yorimoto's EEPROM) are prone to be defective,

c memory patching allows fault tolerance for defect in memory locations, and

d Yorimoto teaches usage of good memory location instead of defective memory location.

6. Claims 92, 116, 118-120, 122, 123, 125-127 are rejected under 35 U.S.C. § 103 as being unpatentable over Burke (AU-B-22536/83) in view of Yorimoto et al. (0-220-718 hereinafter referred to as Yorimoto).

As per claim 92:

Burke teaches a memory system that is connected to a host computer and is comprising: (a) a semiconductor memory; and (b) electronic control means, which is connectable to said computer, for controlling operation of the semiconductor memory. Burke 's semiconductor memory reads on Applicant's array of memory cells. Burke 's electronic control means reads on Applicant's means for controlling the operation the array. Burke 's electronic control means includes circuit means, which reads on Applicant's means for

addressing, for translating address signals, which are from the host computer for the magnetic memory device, to corresponding address signals for the semiconductor memory.

Burke, however does not explicitly teach that his semiconductor memory is of "non-volatile floating-gate" type. Burke also does not explicitly cite that his memory cells are partitioned into a plurality of sectors that individually include a distinct group of memory cells that are erasable together as a unit. Furthermore Burke does not explicitly cite that his memory cells are for storing a given amount of user data and overhead data. Burke does not explicitly cite that his address signals, which are from the host computer for the magnetic memory device, are sector address signals. Burke also does not explicitly recite that his corresponding address signals are addressing a corresponding nonvolatile memory sector. Burke also does not explicitly teach means for reading the overhead data stored in the addressed sector, and means responsive to the read overhead data for executing an instruction from the host computer system to perform a designated one of reading user data from, or writing user data to the addressed sector. But Burke does teaches that his memory system has reading/writing means.

It is understood that (a) Burke's address signals, which are from the host computer for the magnetic memory device, are sector address signals, and (b) Burke's corresponding address signals, which have been derived from translating the sector address signals, are equivalent to that of sector address signals because Burke's semiconductor memory is emulating his magnetic memory device. It is also understood that Burke's memory cells are being partitioned into a plurality of sectors, each of which includes a distinct group of memory cells that are erasable together as a unit, because Burke's semiconductor memory is emulating his magnetic memory device. Besides this understanding, partitioning of nonvolatile

memory cells into a plurality of nonvolatile memory sectors that individually include a distinct group of memory cells that are erasable together as a unit is known in the art (see Yorimoto example),

Official notice is, hereby, taken that: (1) providing, in a sector, enough memory cells for storing a given amount of user data and overhead data; (2) means for reading the overhead data stored in the addressed sector; and (3) means responsive to the read overhead data, (such as validity check bit information, or remapping information), for reading user data from or writing user data to the user data field of the sector, which has the overhead data field in which the overhead data is stored, are notoriously old and well known in the art.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to:

a. realize that Burke's address signals, which are from his host computer for addressing his magnetic memory device, are sector address signals **because** magnetic memory devices are addressed according to sectors;

b. realize that Burke's corresponding address signals, which have been derived from translating the sector address signals, are equivalent to that of sector address signals **because** a translating of one identify must be equivalent to that identify and because Burke's semiconductor memory is emulating his magnetic memory device and those signals which are applied to the emulating device are equivalent to those signals which are applied to the emulated device;

c. realize that Burke's memory cells are being partitioned into a plurality of sectors **because** his memory cells are emulating his magnetic memory device's bit-storing units;

d. realize that each of Burke's information bits in a group of his memory cells are erasable together as a unit **because** Burke's semiconductor memory is emulating his magnetic memory device and it is known in the art that the information bits in a group of bit-storing units (called sector) in a magnetic memory device are erasable together as a unit;

e. replace Burke's semiconductor memory device with nonvolatile memory device, such as that of Yorimoto, **because** nonvolatile memory device would emulate magnetic memory device better since magnetic memory device is nonvolatile;

f. provide, in a sector, enough memory cells for storing a given amount of user data and overhead data **because** otherwise the sector would not able to store all of the necessary amount of information which is to be stored in that sector;

g. provide means for reading the overhead data stored in the addressed sector **because** this overhead data is needed first in order to determine whether the user data in the user data fields are valid or not and whether any field has been remapped; and

h. provide means, responsive to the read overhead data (such as validity check bit information, or remapping information), for reading user data from (or writing user data to) the user data fields of the sector, which has the overhead data field in which the overhead data is stored **because** the objective of accessing

the emulating semiconductor memory device is to read data from or to write data to it.

The artisan would have been motivated to realize the points indicated above because Burke the usage of semiconductor memory device for emulating a magnetic memory device. The artisan would have also been motivated to replace Burke's semiconductor memory device with Yorimoto's nonvolatile memory device because Yorimoto's nonvolatile memory device is capable of being partitioned into sectors which would be suitable for simulating the sectors of a magnetic memory device and suitable for simulating the nonvolatile characteristic of the magnetic memory device. The artisan would also have been motivated to provide the appropriate means in order to properly read information from or write information to the appropriate sector field in the addressed sector because properly read information from and write information to memory device by using overhead information such as error/validity bit information and/or remap information are known in the art of memory fault detection and correction.

As per claims 116 and 123:

Burke's memory system, being connected to his host computer, has electrical terminations for establishing a connection with the host computer. Burke's controller, which is in his memory system, is connected to his host computer. From this connection, it is readily understood that Burke's controller is connected between his electrical terminations and his memory cell array.

As per claim 118:

Official notice is, hereby, taken that storing addresses, which indicate substitute usable memory location, together with other header information such as defect indicating flag is

notoriously old and well known in the art of address translation for the purpose of substituting alternative memory location for defective main memory location.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to the identify unusable sectors and identify, by using address information, the substitute usable sectors so that when an unusable sector is accessed it can be substituted with a usable sector.

One having ordinary skill in the art would be motivated to store the addresses of alternative sector in the header information field because these addresses would refer an access to a substitute memory location and because Yorimoto teaching does relate to substitution of defective memory sector.

As per claim 119:

Yorimoto teaches that unusable memory sectors are those sectors which are defective.

As per claim 120:

Official notice is, hereby, taken that it is notoriously old and well known in the art to identify a bad group of cells, when the number of defective memory cells within the group of cells is greater than a preset number and the number of bit errors in the group of cells is beyond the capability of correcting by using error correction code, so that this group of cells can be replaced with an alternative group of cells.

As per claim 122:

The technique of verifying the validity of addressing a memory location as claimed in this claim is notoriously old and well known in the art of memory accessing checking.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to check whether addressing is valid or not because getting incorrect data

from a memory could be caused by accessing a wrong location due to the error in the address information.

As per claim 125:

Official notice is, hereby, taken that distribution of the segments of a large file among a plurality of memory sectors is notoriously old and well known in the art of storing information. Official notice is also, hereby, taken that it is notoriously old and well known that upon erasing the large file, which has been distributed among a plurality of memory sectors, the plurality of memory sectors must be selected and erased in order for the large file to be completely erased.

As per claim 126:

It would have been obvious to an artisan in the art at the time the invention was made to implement Burke's memory system in a single printed circuit card because the advancement in the technology of semiconductor has encouraged artisans to implement many components of a system into a single printed circuit card so as to modularize the system and to have a more compact unit of the system.

As per claim 127:

Burke's memory system emulates a magnetic memory and translates the address addressing the magnetic memory in order to address the emulating semiconductor memory.

7. Claims 93-97, 117, 121, 124 are rejected under 35 U.S.C. § 103 as being unpatentable over Burke (AU-B-22536/83) and Yorimoto (JP0-220-718) as applied to claims 92 and 116 above, and further in view of Nozawa et al (4,525,839 hereinafter referred to as Nozawa).

As per claims 93 and 117:

In a memory system, Nozawa teaches means (i.e. pointers 23a) listing any unusable ones of a plurality of non-volatile memory sectors for linking the unusable sectors with others of sectors that are usable. Nozawa also teaches, in non-volatile memory-sector addressing means, means (elements 50, 51, 61, 64, 63, 71, 76, and 77) for accessing linked others of said sectors in place of said unusable sectors.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to: (1) use, in Burke's memory system, Nozawa's pointer linking least means for listing memory sector, which cannot be used due to defect, so that the pointers in this pointer linking least means can refer the accessing to an alternate sector which can be used; and (2) provide, in Burke's memory system, Nozawa's means for accessing the alternate sector in place of the defective sector.

The artisan would have been motivated to utilize Burke's pointer linking list means and provide the means for accessing the alternate sector in Burke's memory system because memory patching by method of remapping is notoriously old and well known in the art and because Yorimoto's memory in Burke's modified memory system is prone to be defective and utilization and the provision would provide tolerance to that defect.

As per claims 94 and 124:

The size of 512-bytes, which is took as a given amount of user data, is of obvious design choice.

As per claim 95:

Head, cylinder and sector are well known information fields which are associated with addresses for addressing magnetic disk sector.

As per claims 96 and 121:

Nozawa teaches accessing alternative blocks for defective blocks upon detection of defect in the defective block, thus suggests a controlling means for controlling a substitution.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide, for the purpose of sufficiency, enough redundant memory cells in order to adequately store those information which cannot be stored in the main cells in case the main cells become defective.

As per claim 97:

Official notice is, hereby, taken that header information including defect descriptor comprising defect pointer, which is referred to in order to skip bad memory location and jump to an alternative location for the purpose of replacing the bad memory location is notoriously old and well known in the art.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to realize that it is necessary to provide a referencing means in order to refer to the overhead data (i.e. the defect pointer) in order to determine whether or not the main memory cells need substitution.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ly Hua whose telephone number is (703) 305-9684. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel, Jr., can be reached on (703) 305-9713. The fax phone number for this Group is (703) 305-9600.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-9724.

L. Hua
November 9, 1995

ROBERT W. BEAUSOLIEL, JR.
SUPERVISORY PATENT EXAMINER
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